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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,085	01/27/2004	Keith W. Holt	03-2143	2432

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EXAMINER	
WACHSMAN, HAL D	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,085	HOLT ET AL.	
	Examiner	Art Unit	
	Hal D. Wachsman	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-20* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This application is in condition for allowance except for the following formal matters:

a) The drawings are objected to because Figure 1 refers to block 104 as "FIRST FUNCTIONAL CIRCUIT". However, page 1 of the specification indicates that block 104 is the second functional circuit. Appropriate correction is required.

b) The Abstract is objected to because it contains purported merits (i.e. "without requiring active circuits on the interconnect board"). Appropriate correction is required.

c) Page 1, second paragraph, cites "...to determine other systems contain... "which it appears should be "...to determine other systems containing..". Page 7, line 15, has a period after "402" however that is not the end of the sentence. Appropriate correction is required.

d) PALM is showing an Information Disclosure Statement for the application being filed 2-11-04 however there is no IDS in the image file wrapper. If the Applicant did file an IDS on 2-11-04, the Applicant is respectfully requested to resubmit this IDS with copies of any references that were originally sent in for proper consideration. If no previous IDS was filed, confirmation of that is respectfully requested.

e) Claims 1-7, 9 and 14-20 are objected to under 37 C.F.R. 1.75(a) for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 1, line 3, cites "a first functional signal path" however in this claims and all the claims that depend from claim 1 there is no "second functional signal path". This same type of problem also occurs with respect to "a first functional

signal" in claim 1, line 4 and claim 17, lines 6-7. Claim 1, line 13, cites "the signal" however the antecedent basis is "first functional signal". Claim 2, line 5, cites "the selection signal input path" which lacks antecedent basis. Claim 3, lines 3-4, cite "..to select the latched output signal of the transparent latch to be applied to the output of transparent latch..." which is confusing as to how the output signal of the transparent latch is being applied to its own output at the transparent latch. Claim 3, lines 4-5, cite "the functional circuits of the second circuit board" which lacks clear antecedent basis. The preambles of claims 4-7 cite "The system..." which it appears should be "The test system...". Claim 5, line 1, cites "..wherein functional signal..." which it appears should be "said functional signal". A period is missing at the end of claim 9. Claim 14, line 3, cites "the functional signal paths" which it appears should be "the first and second functional signal paths". Claim 15, line 1, cites "the out of band signals" which it appears should be "the out of band test signals". This same type of problem also occurs in claim 16, line 1. Claim 15, line 2, cites "the band of modulated functional signals" which lacks clear antecedent basis. Claim 16, line 2, cites "the band of encoded functional signals" which lacks clear antecedent basis. Claim 19, lines 2-3, cite "the normal band of modulation of the functional signals" which appears to lack clear antecedent basis. Claim 20, line 2, cites "the functional signals" however the antecedent basis is singular. The last 2 lines of claim 17 cites "using the latched present state of the first functional signal within the second circuit board during the exchange of test signal" but for what exactly within the second circuit board is the latched present state being used for ? The examiner asks the applicant to better claim the limitations cited above. While the

examiner understands the intentions of the applicant he feels confusion could be drawn from the limitations cited above. Appropriate correction is required.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

2. The following references are cited as being art of general interest: Henry et al. (EP 1 271 334 A2) which disclose a high bandwidth storage device controller architecture and RAID, Oldfield et al. (US 2002/0133740 A1) which disclose a redundant controller data storage system for handling controller resets and Schaber et al. (US 2002/0170006) which disclose a differential receiver architecture.

3. Claims 1-7 are allowable over the prior art because the prior art does not disclose or suggest: a first test control circuit in a first circuit board coupled to a test signal path, which is for exchanging test signals between the first circuit board and a second circuit board, the first test control circuit adapted to apply a test request signal to the test signal path; and a second test control circuit in the second circuit board coupled to a functional signal path and coupled to the test signal path and adapted to latch the present state of the functional signal on a functional signal path for use within the second circuit board in response to receipt of the test request signal from the first circuit board.

Claims 8-16 are allowable over the prior art because the prior art does not disclose or suggest: first test control logic in a first circuit board coupled to a test signal means and coupled to a second of two functional signal paths for latching the present state of a second of two functional signals within the first circuit board during testing of the second functional signal path; second test control logic in a second circuit board coupled to test signal means and coupled to a first of two functional signal paths for latching the present state of a first of two functional signals within the second circuit board during testing of the first functional signal path, wherein the first test control logic is operable to latch the present state of the second functional signal in response to a test request signal received from the second test control logic through the test signal means.

Claims 17-20 are allowable over the prior art because the prior art does not disclose or suggest: applying a first test request signal from a first circuit board to a second circuit board wherein the first test request signal is out of band with respect to a cross-coupled signal pair coupled between the first circuit board and a second circuit board and latching within the second circuit board the present state of a functional signal of the cross-coupled signal pair in response to detection of the first test request signal with the exchange of test signals between the two circuit boards to test the signal path for the functional signal.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal D. Wachsman whose telephone number is 571-272-

2225. The examiner can normally be reached on Monday to Friday 7:00 A.M. to 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hal D Wachsman
Primary Examiner
Art Unit 2857

HW
April 16, 2005